In the Claims

Please cancel claims 1-20

Please add claims 21-40.

21. (New) A non-stalled cache system, coupled to a memory module adapted to store a plurality of memory blocks, the system comprising:

a cache module, coupled to the memory module, adapted to store a first memory block of the plurality of memory blocks;

an address module adapted to receive a first pixel identifier of a plurality of pixel identifiers and adapted to determine whether the first pixel identifier corresponds to the first memory block stored within the cache module; and

a controller module, coupled to the cache module and the address module, adapted to respond to the first pixel identifier corresponding to the first memory block by synchronizing the non-stalled transmission from the cache module of a first texel within the first memory block and the non-stalled storage of a second memory block of the plurality of memory blocks from the memory module in the cache module; said first texel corresponding to the first pixel identifier.

22. (New) The system of claim 21 wherein the address module further comprises:

an address controller, coupled to the memory module and the controller module, adapted to respond to the first pixel identifier corresponding to the first memory block stored within the cache module by transmitting a first transmit tag signal to the controller module; said address

module adapted to respond to the first pixel identifier not corresponding to the first memory block stored within the cache module by transmitting a retrieval signal to the memory module and a retrieval tag signal and a second transmit tag signal to the controller module; said retrieval signal triggering the transmission of a second memory block of the plurality of memory blocks from the memory module; said first transmit tag signal corresponding to the first texel within the first memory block within the cache module; said second transmit tag signal corresponding to a second texel within the second memory block that is to be stored within the cache module; said retrieval tag signal corresponding to the second memory block to be stored within the cache module.

23. (New) The system of claim 21 wherein the address module further comprises:

a tag module adapted to store an association between the first pixel identifier and a cache block address; said cache block address representing the location of the first memory block within the cache module.

24. (New) The system of claim 21 wherein the address module further comprises:

a tag reference counter adapted to increment a value by one when the first pixel identifier corresponds to the first memory block within the cache module; said value representing a number of consecutively received pixel identifiers of the plurality of pixel identifiers corresponding to one of the plurality of memory blocks stored within the cache module.

3 26. (New) The system of claim 22 wherein the controller module further comprises:

a retrieval controller, coupled to the address controller, adapted to respond to receipt of the retrieval tag signal from the address controller by synchronizing the non-stalled transfer of the second memory block from the memory module into the cache module to ensure that one of the plurality of memory blocks already within the cache module is not prematurely overwritten.

4 27. (New) The system of claim 22 wherein the controller module further comprises:

a data reference counter adapted to increment a value by one when the controller module triggers the transmission of the first texel from the cache module; said value representing a number of consecutive texels corresponding to the first transmit tag signal that are triggered to be transmitted from the cache module.

5 28. (New) The system of claim 22 wherein the controller module further comprises:

a transmit controller, coupled to the address controller and the cache module, adapted to respond to the receipt of the first transmit tag signal from the address controller by triggering the transmission of the first texel from the cache module and adapted to respond to receipt of the second transmit tag signal from the address controller by triggering the transmission of the second texel from the cache module.

28. (New) The system of claim 21 wherein the controller module further comprises:

a status module adapted to store a logic state for the cache module; said logic state corresponding to a read logic state or a write logic state.

29. (New) The system of claim 21 further comprising:

a data formatter, coupled to the memory module and the cache module, adapted to receive data in a first format from the memory module and to transmit the data in a second format to the cache module.

30. (New) A non-stalled cache system, coupled to a cache module and a memory module, the system comprising:

a data reference counter adapted to respond to the triggering of transmission of a first texel of a first memory block from the cache module by incrementing a first value by one; said first memory block is one of a first plurality of memory blocks stored within the cache module; said first value representing a number of consecutive texels from at least one of the first plurality of memory blocks within the cache module that are triggered to be transmitted from the cache module; and

a retrieval controller, coupled to the data reference counter, adapted to respond to the first value having a value at least equal to a second value by triggering the storing of a second memory block of a second plurality of memory blocks from the memory module in the cache

module; said second value representing a number of consecutive texels corresponding to a first transmit tag signal.

31. (New) The system of claim 30 further comprising:

a transmit controller, coupled to the retrieval controller and the cache module, adapted to respond to the receipt of a first transmit tag signal by triggering the transmission of the first texel from the cache module and adapted to respond to receipt of a second transmit tag signal by triggering the transmission of a second texel of the second memory block from the cache module.

32. (New) A method for non-stalled caching of at least one of a plurality of memory blocks from a memory module, the method comprising the steps of:

storing a first memory block of the plurality of memory blocks in a cache module;

determining whether a first pixel identifier of a plurality of pixel identifiers corresponds to the first memory block within the cache module; and

responding to the first pixel identifier corresponding to the first memory block by synchronizing the non-stalled transmission from the cache module of a first texel within the first memory block from the cache module and the non-stalled storage of a second memory block of the plurality of memory blocks from the memory module in the cache module.

33. (New) The method of claim 32 wherein the determining step comprises the additional steps of:

responding to the first pixel identifier corresponding to the first memory block stored within the cache module by transmitting a first transmit tag signal to a controller module; and

responding to the first pixel identifier not corresponding to the first memory block within the cache module by transmitting a retrieval signal to the memory module and a retrieval tag signal and a second transmit tag signal to the controller module; said retrieval signal triggering the transmission of a second memory block of the plurality of memory blocks from the memory module; said first transmit tag signal corresponding to the first texel within the first memory block within the cache module; said second transmit tag signal corresponding to a second texel within the second memory block that is to be stored within the cache module; said retrieval tag signal corresponding to the second memory block to be stored within the cache module.

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34. (New) The method of claim 32 wherein the determining step comprises the additional step of:

storing an association between the first pixel identifier and a cache block address; said cache block address representing the location of the first memory block within the cache module.

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35. (New) The method of claim 32 wherein the determining step comprises the additional step of:

generating a value representing a number of consecutively received pixel identifiers of the plurality of pixel identifiers corresponding to one of the plurality of memory blocks within the cache module.

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36. (New) The method of claim 33 wherein the step of responding to the first pixel identifier corresponding to the first memory block comprises the additional step of:

responding to receipt of the retrieval tag signal by synchronizing the non-stalled transfer of the second memory block from the memory module into the cache module to ensure that a memory block within the cache module is not prematurely overwritten.

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37. (New) The method of claim 33 wherein the step of responding to the first pixel identifier corresponding to the first memory block comprises the additional step of:

incrementing a value by one when a controller module triggers the transmission of the first texel from the cache module; said value representing a number of consecutive texels corresponding to the first transmit tag signal that are triggered to be transmitted from the cache module.

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38. (New) The method of claim 32 wherein the step of responding to the first pixel identifier corresponding to the first memory block comprises the additional step of:

storing a logic state for the cache module; said logic state corresponding to a read logic state or a write logic state.

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39. (New) The method of claim 32 wherein the step of responding to the first pixel identifier corresponding to the first memory block comprises the additional step of:

responding to the triggering of transmission of the first texel of the first memory block from the cache module by incrementing a first value by one; said first memory block is one of

the plurality of memory blocks stored within the cache module; said first value representing the number of consecutive texels from at least one of the plurality of memory blocks within the cache module that have been triggered to be transmitted from the cache module.

40. (New) The method of claim 32 wherein the step of responding to the first pixel identifier corresponding to the first memory block further comprises the additional step of:

responding to a first value having a value at least equal to a second value by triggering the storing of the second memory block of the plurality of memory blocks from the memory module in the cache module; said first value representing a number of consecutive texels corresponding to the first transmit tag signal that are to be transmitted from the cache module; said second value representing a number of consecutively received pixel identifiers of the plurality of pixel identifiers corresponding to one of the plurality of memory blocks within the cache module.

REMARKS

Claims 1-20 were presented for examination.

Claims 1-20 were rejected.

Figure 3 was revised to correct informalities in the originally filed drawing.

Claims 1-20 are canceled.